Claims

What is claimed is:

1. A system for protecting an integrated circuit from electrostatic discharge, the system comprising:

a core region;

a pad electrically coupled to the core region through an input device, the input device having at least one CMOS device with a gate oxide layer; and

at least one protection diode operable to provide a discharge path for electrostatic discharge due to a high voltage being applied to the pad wherein the at least one protection diode has a reverse breakdown voltage less than the breakdown voltage of the gate oxide layer.

2. The system of claim 1, the reverse breakdown voltage of the at least one diode being greater than the supply voltage and less than the breakdown voltage of the gate oxide layer.

3. The system of claim 2, the reverse breakdown voltage of the at least one diode being determined by the equation V_{CC} +2V < B_{VR} < Bvox where V_{CC} is the supply voltage, Bvox is the breakdown voltage of the gate oxide layer and B_{VR} is the reverse breakdown voltage of the at least one diode.

4. The system of claim 1, the at least one diode comprising a first diode and a second diode forming an input protection circuit adapted to protect the input device.

5. The system of claim 1, the at least one diode comprising a power supply clamp diode.

6. The system of claim 1, the at least one diode comprising a heavily doped N^{++} region and a heavily doped P^{++} region.

7. The system of claim 1, the input device being a CMOS inverter formed from a PMOS and an NMOS transistor.

8. The system of claim 1, the core region comprising a flash memory device.

9. A method of forming a diode for protecting an integrated circuit from electrostatic discharge, the integrated circuit being formed on a substrate having a core region, a pad electrically coupled to the core region through an input device having at least one CMOS device with a gate oxide layer, the method comprising:

forming a heavily doped N^{++} cathode region in a peripheral region of the substrate;

forming a heavily doped P^{++} anode region adjacent the cathode region, the cathode region and the anode region forming a diode; and

wherein the reverse breakdown voltage of the diode is less than the breakdown voltage of the gate oxide layer.

10. The method of claim 9, the diode being formed in a guard ring of the integrated circuit.

11. The method of claim 9, further comprising forming a contact from the cathode region through a dielectric layer and connecting the contact to a supply voltage.

12. The method of claim 11, the reverse breakdown voltage of the diode being greater than the supply voltage.

13. The system of claim 12, the reverse breakdown voltage of the diode being determined by the equation $V_{CC} + 2V < B_{VR} <$ Bvox where V_{CC} is the supply voltage, Bvox is the breakdown voltage of the gate oxide layer and B_{VR} is the reverse breakdown voltage of the diode.

14. The method of claim 11, the anode being connected to a second supply through the substrate.

15. The method of claim 11, the substrate being a p-type substrate.

16. The method of claim 15, the diode being formed from a P^+ implant in the peripheral region of the p-type substrate to form a heavily doped P^{++} region and at least one N^+ implant in the heavily doped P^{++} region.

17. The method of claim 16, the at least one N^+ implant comprising a first N^+ implant in the heavily doped P^{++} region to form a N^+ region and a second N^+ implant into the N^+ region to form the heavily doped N^{++} cathode region.

18. The method of claim 17, the first N^+ implant having a dose in the range of about $1x10^{14}$ to about $1x10^{16}$ atoms/cm^2 and implanted at an energy range of about 50KeV to about 70 KeV and the second N^+ implant having a dose in the range of about $1x10^{13}$ to about $1x10^{15}$ atoms/cm^2 and implanted at an energy level within the range of about 50 KeV to about 70 KeV.

19. The method of claim 16, the P^+ implant having a dose in the range of about $1x10^{12}$ to about $1x10^{15}$ atoms/cm^2 and implanted at an energy range of about 30KeV to about 50 KeV.

20. The method of claim 9, the diode being formed as part of the formation of a flash memory device.

21. A method of forming a flash memory device with at least one protection diode for protecting the flash memory device against electrostatic discharge, the flash memory device having an input device coupling the flash memory cells to at least one pad, the input device having at least one CMOS device with a gate oxide layer, the method comprising;

providing a substrate having a core region and a peripheral region;

selectively opening core implant masks at the peripheral region of the mask, so that at least one protection diode can be formed concurrently with the flash memory cells;

performing a plurality of core implants to form flash memory cells in the core region of the substrate and the at least one protection diode in the peripheral region of the substrate;

wherein core implants are selected to provide the at least one protection diode with a reverse breakdown voltage less than the breakdown voltage of the gate oxide layer.

22. The method of claim 21, the selected core implants being two of a core implant, a double diffused implant and a medium doped drain implant.

23. The method of claim 21, the core implants are selected to provide a reverse breakdown voltage of the diode that is determined by the equation V_{CC} +2V < B_{VR} < Bvox where V_{CC} is the supply voltage, Bvox is the breakdown voltage of the gate oxide layer and B_{VR} is the reverse breakdown voltage of the diode.

24. The method of claim 21, the diode being formed in a guard ring of the flash memory device.